ABSTRACT

A buffer logic within a memory module having the capability to carry out a test of another memory module to which it is coupled via a point-to-point bus through autonomously storing and transmitting a test pattern across that point-to-point bus to the other memory module, while further employing another buffer logic that is interposed between the two memory modules to pass on the test pattern, but intercept a signal received from the other memory module during the test and pass on an indication of the receipt of that signal to an analysis device to monitor the test.